SDR Zero-IF Transceiver

DSP Project Presentation

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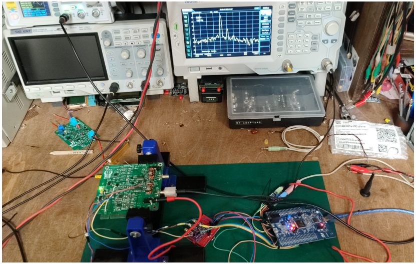


Modulation

Modulation

Process of varying one or several parameters of a periodic carrier signal. Allows for easier transmission and processing of a baseband signal.

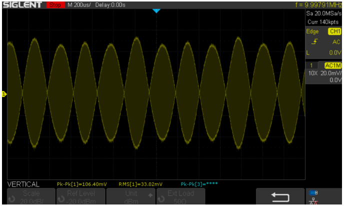
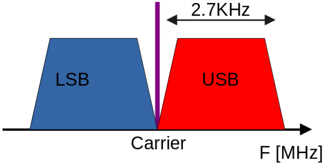


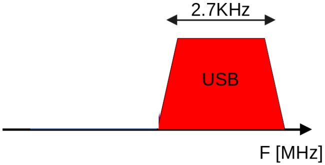
Figure: Amplitude modulation in time domain

Easiest form of modulation is amplitude modulation.
Modulating signal is of lower frequency than a carrier.
If a sinewave of frequency f_m modulates carrier f_c then 3 peaks are observed at: $f_c - f_m$, f_c, $f_c + f_m$

AM-Single Side Band



(a) Amplitude Modulation



(b) Single Sideband

Figure: Spectrum of two modulation schemes

In AM modulation the lower and upper sideband (LSB/USB) contain the same information.
Carrier contains no information.
Traditional AM is limited to 33% of power spectral efficiency.
SSB conveys the same information using half the bandwidth and increases efficiency.

SSB characteristics

SSB is good for a long distance direct voice communication with narrow bandwidth (military, government services, emergency relief effort, amateur radio).

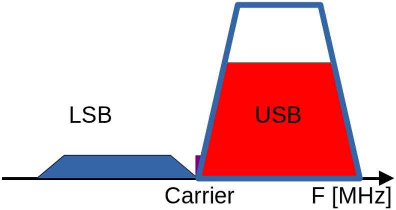


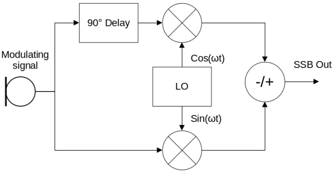
Figure: Realistic spectrum of upper sideband SSB transmission

SSB has some drawbacks:

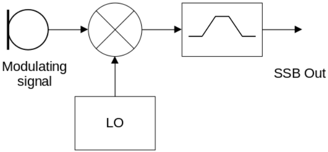
- More difficult to modulate and demodulate
- Difficult to tune ("Donald Duck effect")

Methods of SSB modulation and demodulation

There are two main methods of SSB implementation:



(a) Phase method



(b) Filter method

Figure: Spectrum of two modulation schemes

Filter method is very intuitive but requires narrow filter.

Phase method requires phase matching.

Modern SSB transceivers

In past few years manufacturers in amateur radio have switched to SDR architectures.
Both direct and mixed architectures can be found on the market.

Figure: Xiegu G90 is an example of zero-IF SDR HF transceiver

General architectures of SDR RF receiver

In SDR software performs the extraction of information but the signal has to be conditioned by analog front end first.

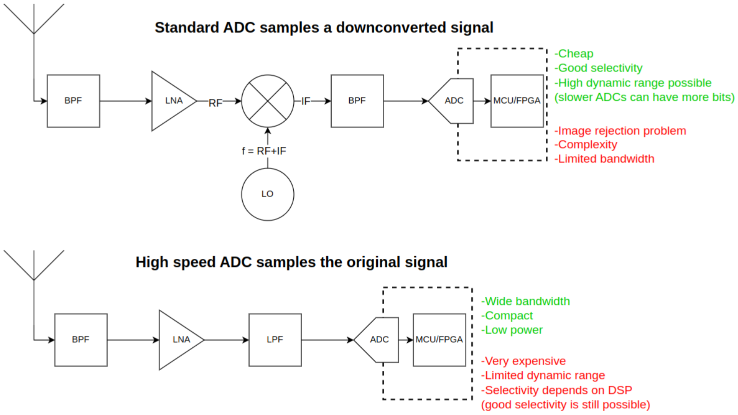


Figure: Two distinct approaches to SDR front ends

Zero-IF architecture

What if we set the LO frequency to received RF frequency?

Zero-IF architecture

What if we set the LO frequency to received RF frequency?

Then carrier will be down converted to DC, this is fine for symmetrical modulation (ex. AM) but what about others?

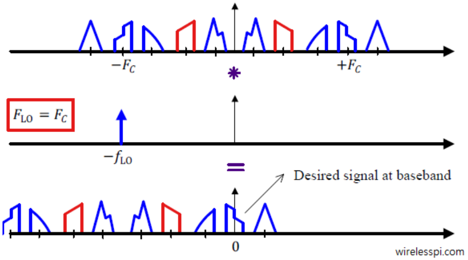


Figure: Spectrum view of LO=FC conversion
source: Wirelessspi direct conversion zero-IF, access 18.01.2024

Zero-IF uses complex signals to overcome this issue with math! Zero image rejection in sight.

Block diagram of the IQ board - RX path

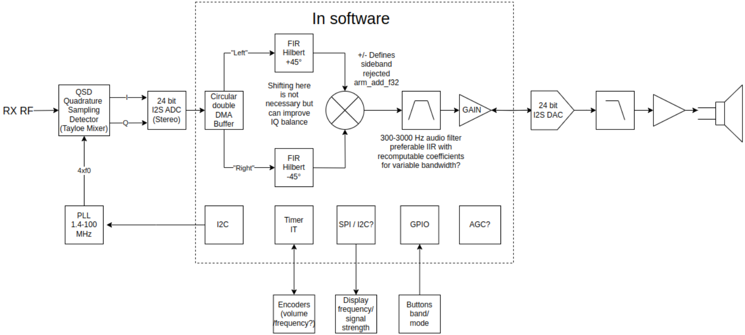


Figure: Block diagram of the prototype in the receive mode

Notice that zero-IF implementation is very close to the phasing method - the original method that SSB was created in early 1940s before mechanical crystals were narrow enough.

Schematic of RX path

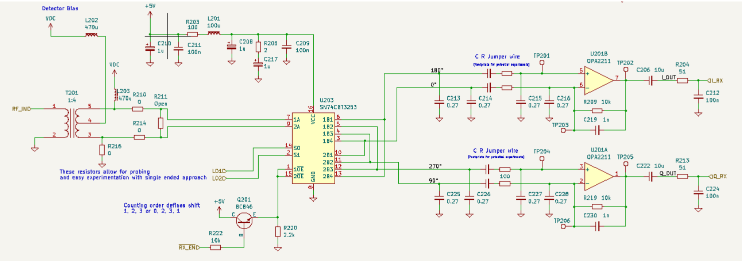


Figure: Schematic of Tayloe IQ decoder

Block diagram of the IQ board - TX path

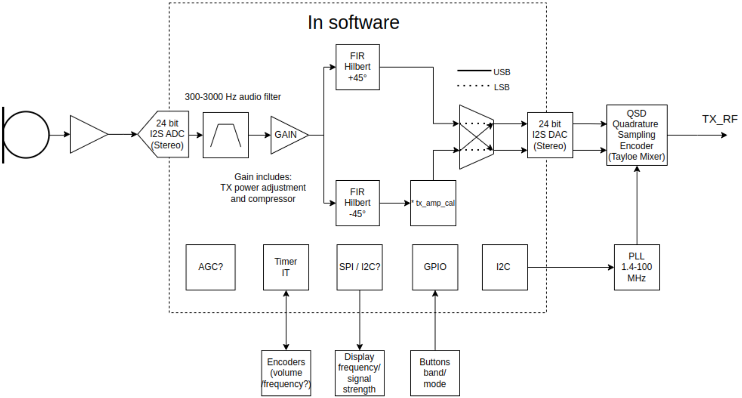


Figure: Block diagram of the prototype in the receive mode

Schematic of TX path

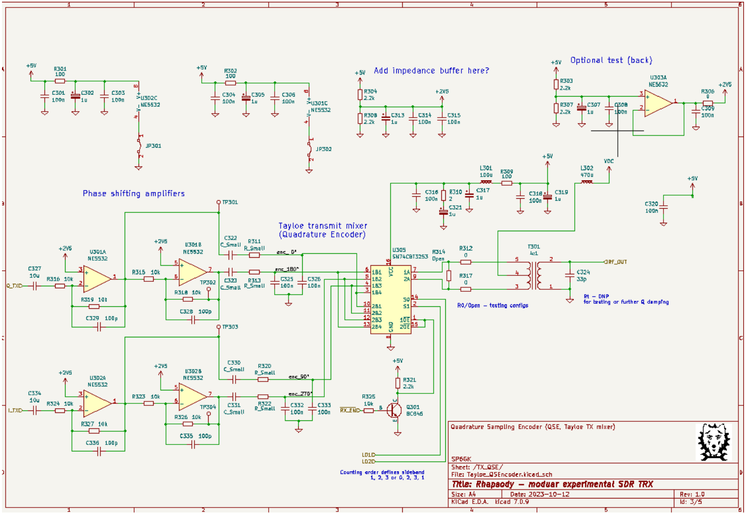
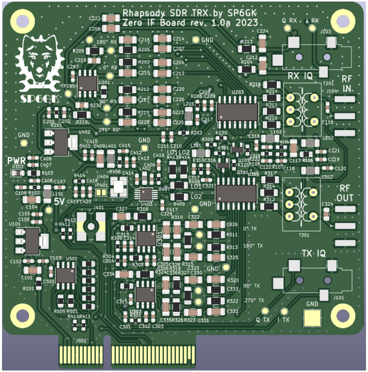


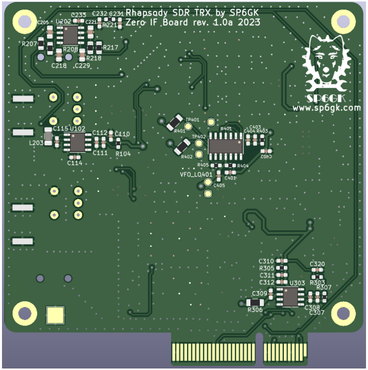
Figure: Schematic of Tayloe IQ encoder

PCB

Goal is to create a modular amateur radio transceiver. This PCB was designed as a module that follows either heterodyne IF or a bank of BPFs.



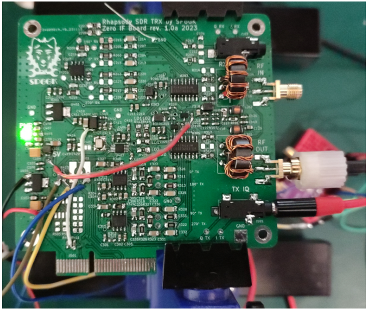
(a) front



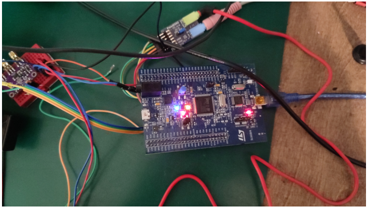
(b) back

Figure: Designed PCB

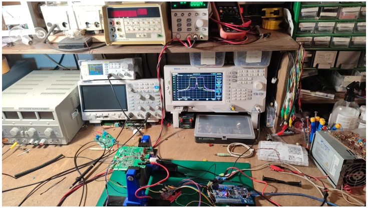
Some photos



(a) IQ board (detector, encoder, PLL VFO)



(b) MCU (discovery, ADC+DAC)



(c) Testing setup

Figure: Photos taken during development

MCU, I2S

Code runs on STM32F407 with clock of 168 MHz. Pmod I2S2 devboard contains CS5343 ADC and CS4344 DAC. Resolution is 24 bits, samples are contained in 32 bit floats. Sampling is 48 KHz.

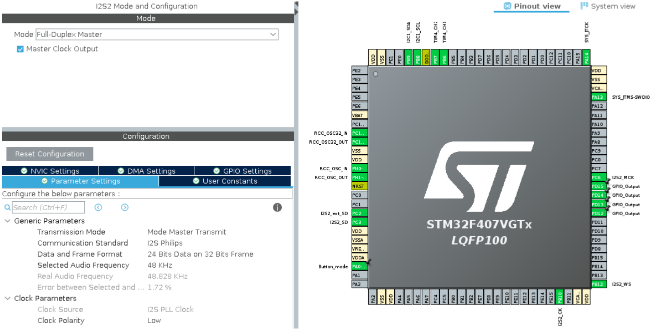


Figure: Cube IDE, pinout view and I2S configuration

Buffers and DMA

Circular ping-pong buffer was implemented.
I2S is used to communicate with ADC and DAC, using DMA callbacks on the halves of the buffer. Whole buffer has 512 float samples. While half of the buffer is filled in the other half is being processed by the CPU.

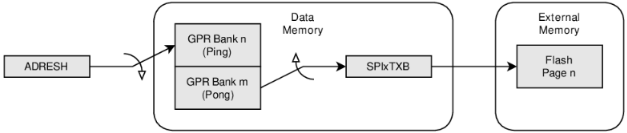


Figure: "Ping-Pong buffer"
source: Microchip onlinedocs, access 18.01.2024

Code - CMSIS DSP (RX processing)

```c
        if (callback_state != 0) {
            //decide if it was half or cplt callback
            if (callback_state == 1)    {
                    offset_r_ptr = 0;
                    offset_w_ptr = 0;
                    w_ptr = 0;
                }
            else if (callback_state == 2) {
                offset_r_ptr = BLOCK_SIZE_U16;
                offset_w_ptr = BLOCK_SIZE_FLOAT;
                w_ptr = BLOCK_SIZE_FLOAT;
            }
            //restore input sample buffer to float array
            for (int i=offset_r_ptr; i<offset_r_ptr+BLOCK_SIZE_U16; i=i+4) {
                l_buf_in[w_ptr] = (float) ((int) (rxBuf[i]<<16)|rxBuf[i+1]);
                r_buf_in[w_ptr] = (float) ((int) (rxBuf[i+2]<<16)|rxBuf[i+3]);
                w_ptr++;
            }
          if(tx_flag == 0){
            //RX path
            HAL_GPIO_WritePin(GPIOD, GPIO_PIN_14, GPIO_PIN_RESET);
            //process FIR +/-45 degree Hilbert
            arm_fir_f32 (&firsettings_l, &l_buf_in[offset_w_ptr], &l_buf_out[offset_w_ptr], BLOCK_SIZE_FLOAT);
            arm_fir_f32 (&firsettings_r, &r_buf_in[offset_w_ptr], &r_buf_out[offset_w_ptr], BLOCK_SIZE_FLOAT);
            arm_scale_f32(l_buf_out, rx_amp_cal, l_buf_out, 1024);
            //summation of two signals 90 degree out of phase.
            if(mode == 1){
                arm_add_f32(l_buf_out, r_buf_out, sum_buf_rl, 1024);
            }
            else{
                arm_sub_f32(l_buf_out, r_buf_out, sum_buf_rl, 1024);
            }
            //Check for overflow. TODO Potentially scale data before?, TODO check if this is necessary (arm_add might
            for (uint32_t i = 0; i < BLOCK_SIZE_FLOAT; i++) {
                    if (sum_buf_rl[i] > FLOAT_MAX) {
                        sum_buf_rl[i] = FLOAT_MAX;
                    } else if (sum_buf_rl[i] < FLOAT_MIN) {
                        sum_buf_rl[i] = FLOAT_MIN;
                    }
                }
            arm_scale_f32(sum_buf_rl, rx_volume, sum_buf_rl, 1024);
            //SSB audio output filter. Removes below 300 Hz to get rid off the Hilbert imperfection,
            arm_fir_f32 (&firsettings_rl_sum, &sum_buf_rl[offset_w_ptr], &audio_out[offset_w_ptr], BLOCK_SIZE_FLOAT);
```

Phase shifting using FIR filters

FIR filters can maintain a linear phase. Hilbert filter can be calculated to add or remove 45° phase shift.

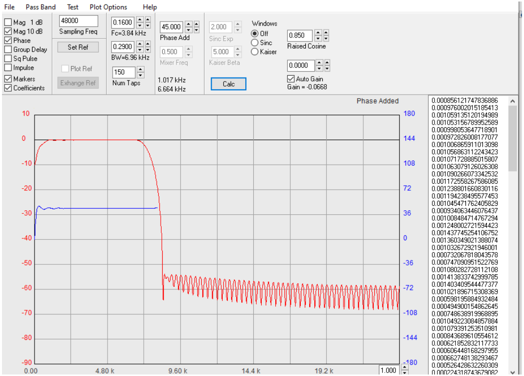
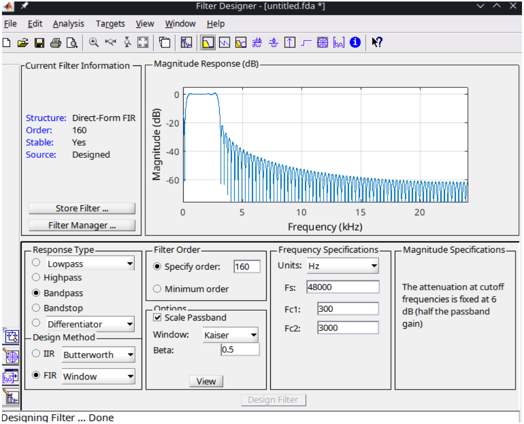


Figure: Iowa Hills Hilbert filter software

A significant trade off has to be made between flatness of phase and lower side magnitude response.

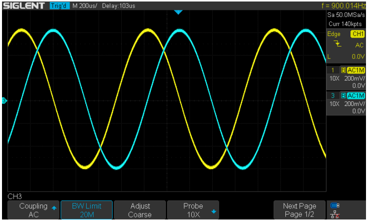
Matlab fdatool



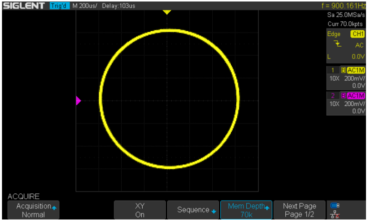
Matlab generated coefficients were used to filter the output and input audio.

Hilbert IQ generation test

Audio was fed to the ADC and IQ signals were output at the DAC. Good 90° phase shift can be seen.



(a) IQ in time domain

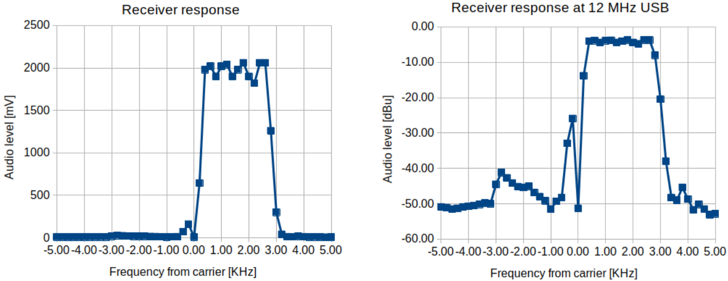


(b) Plot of IQ singals in XY

Figure: Oscilloscope view of the signal processed by the mcu

RX - opposite sideband suppression

Tone was swept across spectrum with center frequency of 12 MHz. Receiver was put in USB mode, audio signal level in mV was noted.



(a) Lin Y scale (b) Log Y scale

Figure: Response of the receiver

This also shows why dB is the preferred unit in RF. Linear scale was converted to dB knowing that the impedance output of the DAC was 10k Ω.

RX measurement

The RX opposite sideband suppression measurement was difficult because:

- This circuit has a lot of gain. I have used NE5532 as a temporary opamp in phase summator. This not a low noise op amp by modern standards.
- Oscilloscope has a very limited dynamic range (8 bits).

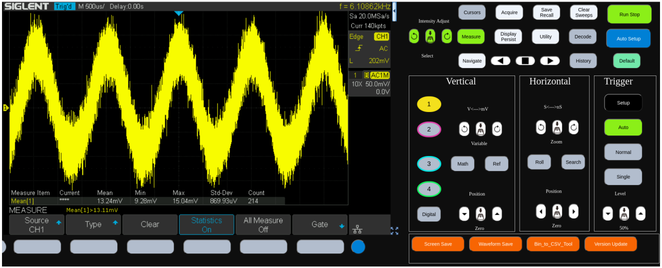


Figure: Oscilloscope remote control view during sideband suppression measurement on receive. High averaging was used, along limited bandwidth.

IQ imbalance - RX optimization

IQ imbalance is major problem in zero IF.
Non ideal 90° phase shift between arms or difference in magnitude will hinder performance.
Tuning variable was added to scale the amplitude in one arm of the signal's path.

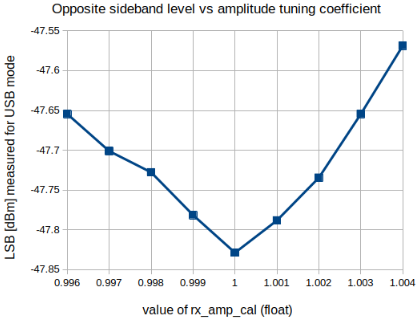


Figure: No improvement was noted as the variable was changed

Only high quality 0.1% tolerance resistors were used and 5% or less tolerance for capacitors.

TX - 1.4 MHz

Used PLL in IQ mode for the Tayloe mixers can work from 1.4-100 MHz. That is also the range that TRX can work in. Transmitter path was tested next since spectrum analyzer has much better dynamic range.

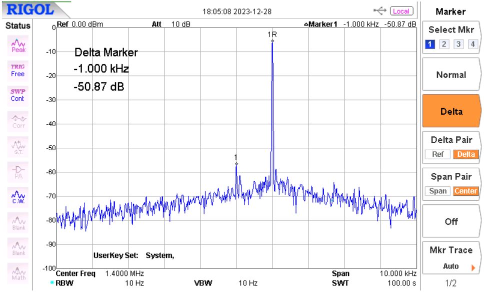
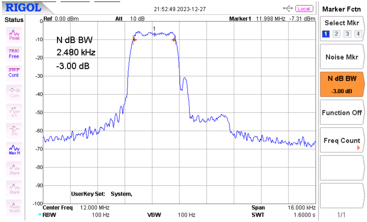


Figure: LSB signal is in the noise floor!

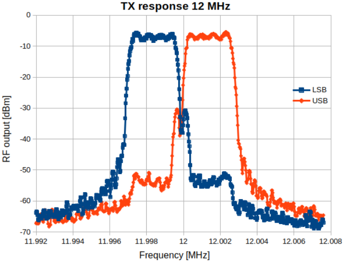
Excellent result, noise around fundamental can most likely be improved with lower noise op amps.

TX - 12 MHz

The same test but for 12 MHz center frequency, the CW input signal was swept. Data was saved to .csv from SA.



(a) 3dB bandpass marker



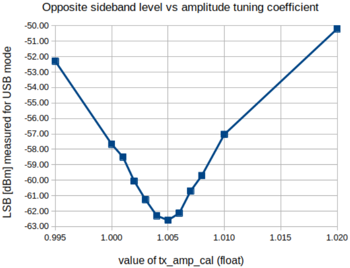
(b) LSB and USB

Figure: Response of the receiver

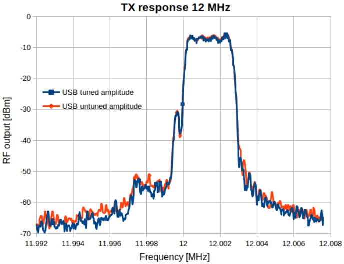
RF level [dBm]	LSB	USB
Fundamental signal	-6.87	-6.3
Carrier suppression	31.16	32.17
Opposite sideband suppression	44.98	44.9

TX - IQ amplitude imbalance tuning

Again the scaling was used on the one arm to improve the suppression.



(a) Tuning of the float variable



(b) Spectrum before and after

Figure: Tuning of the TX IQ amplitude imbalance

Change from 1.0 to 1.005 scaling has improved suppression by more than 4 dB.

TX - 30 MHz

30 MHz (10 m λ) is the end of the amateur radio HF spectrum.

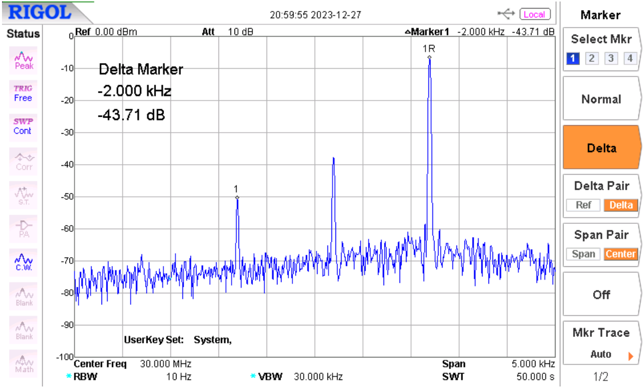
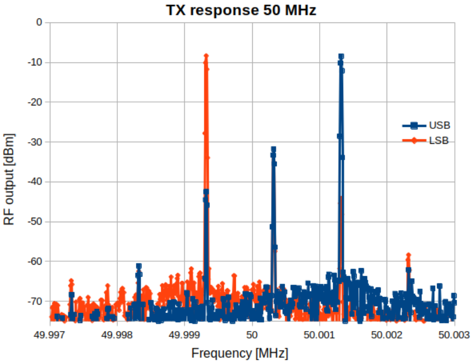


Figure: 30 MHz USB transmitter test

Still good result, but performance is decreasing.

TX - 50 MHz

50 MHz (6m) is first UHF amateur radio band.



RF level [dBm]	USB	LSB
Fundamental signal	-8.43	-8.34
Carrier suppression	23.3	23.37
Opposite sideband suppression	34.06	35.8

Rather poor results, but such wide bandwidth is still impressive.

TX - 100 MHz

Maximal possible frequency with installed PLL (Si5351 in IQ mode) was checked.

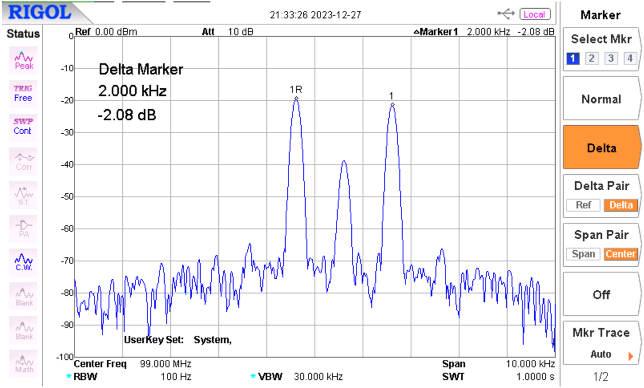
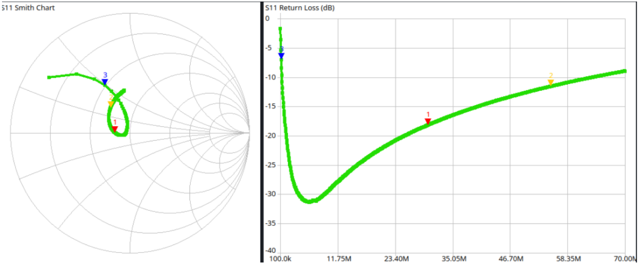


Figure: "SSB" spectrum for 100 MHz

It does not work at all as it should. Most likely due to a poor IQ clock signaling.

Some extras

- Input and output 1:4 transformer have RL $\leq$ 10dB up to 60 MHz. FT50-43 core with 10 bifillar turns was used.



- DC spike was observed when VFO was changing frequency - typical effect in zero-IF, LO leakage mixes with RF (the same frequency) creating a DC.
- I was able to run 3 FIR with 150 coefficients, more coefficients than 160 for each filter required more processing.
- Pull-load effect on the 50Ω ports might change the gain in the op amp section.

Literature

- Experimental Methods in RF Design, SDR chapter
  W.Hayward W7ZOI, R.Campbell KK7B, B.Larkin W7PUA
- Understanding Digital Signal Processing
  Richard Lyons, 1997
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- Ultra Low Noise, High Performance, Zero IF Quadrature Product Detector and Preamplifier
  Dan Tayloe, Link to an article, access 18.01
- A Software-Defined Radio for the Masses, Part 1 Product Detector and Preamplifier
  Gerald Youngblood, AC5OG , Link to a paper, access 18.01
- Direct Conversion (Zero-IF) Receiver
  Wireless Pi, Zero-IF, access 18.01

Other references

- IIR Filters - Audio DSP On STM32 with I2S (24 Bit / 96 kHz)
  YetAnotherElectronicsChannel, Youtube tutorials on STM32 audio DSP
- NA5Y - Youtube channel
  Lots of RF-DSP oriented video blogs
- Charlie Morris ZL2CTM - Youtube channel
  Home made RF projects, including SDR radios
- CMSIS DSP Software Library
  CMSIS-DSP docummentation, keil.com.

The End